WHAT IS CLAIMED IS:

1. A method for aligning an input clock signal with a delay clock signal, the method comprising:

detecting phases of the input clock signal and the delay clock signal to generate a phase detection signal;

detecting edges of the delay clock signal to generate a detect signal;

selecting the delay clock signal or the input clock signal to provide a selection signal in response to the detect signal; and

controlling a delay of the selection signal in response to the phase detection signal to generate the delay clock signal.

2. The method of claim 1 wherein detecting the phases of the input clock signal and the delay clock signal further comprises:

dividing a frequency of the delay clock signal using a first frequency divider to generate a first frequency divided delay signal; and

comparing phases of the input clock signal with the first frequency divided delay signal to generate the phase detection signal using a phase comparator.

3. The method of claim 2 further comprising:

dividing the frequency of the delay clock signal using a second frequency divider to generate an output clock signal.

4. The method of claim 3 further comprising:

providing the output clock signal to programmable circuit elements in a programmable integrated circuit.

5. The method of claim 1 wherein selecting the delay clock signal or the input clock signal to provide the selection signal in response to the detect signal further comprises:

coupling a feedback loop around an adjustable delay circuit to form an oscillator circuit that generates the delay clock signal when the detect signal has a first value that selects the delay clock signal as the selection signal; and

decoupling the feedback loop from an input of the adjustable delay circuit when the detect signal has a second value that selects the input clock signal as the selection signal.

6. The method of claim 1 wherein controlling the delay of the selection signal in response to the phase detection signal to generate the delay clock signal further comprises:

increasing the delay of the selection signal through an adjustable delay circuit when the phase detection signal indicates that an edge of the delay signal is ahead of a corresponding edge of the input signal; and

decreasing the delay of the selection signal through the adjustable delay circuit when the phase detection signal indicates that an edge of the delay signal is behind a corresponding edge of the input signal.

7. The method of claim 1 wherein selecting the delay clock signal or the input clock signal to provide the selection signal in response to the detect signal further comprises:

selecting the delay clock signal as the selection signal regardless of the value of the detect signal when a disable signal has a predefined value.

8. A circuit for aligning a periodic input signal with a delay signal, the circuit comprising:

a phase detector having a first input coupled to the periodic input signal;

an adjustable delay circuit coupled to an output of the phase detector that generates the delay signal at an output of the adjustable delay circuit;

a feedback loop circuit coupled to the output of the adjustable delay circuit;

an edge detector circuit having an input coupled to the output of the adjustable delay circuit; and

a multiplexer having data inputs coupled to the feedback loop and the periodic input signal, a select input coupled to receive a detect signal from the edge detector circuit, and an output coupled to an input of the adjustable delay circuit.

9. The circuit according to claim 8 further comprising:

a first frequency divider circuit having an input coupled to the output of the adjustable delay circuit and an output coupled to a second input of the phase detector, the first frequency divider dividing a frequency of the delay signal by N to generate a divided signal.

10. The circuit according to claim 9 wherein the edge detector circuit generates a HIGH pulse one-half a period of the delay signal before a rising edge of the divided signal.

11. The circuit according to claim 9 wherein the first frequency divider is a counter circuit, and the edge detector circuit generates a HIGH pulse after the counter circuit counts a predetermined number of edges of the delay signal.

12. The circuit according to claim 9 further comprising:

a second frequency divider circuit having an input coupled to the output of the adjustable delay circuit that generates a periodic output signal, wherein the second frequency divider divides a frequency of the delay clock signal by M, and the periodic output signal has a frequency that is N/M times the frequency of the input signal.

13. The circuit according to claim 8 further comprising:

a logic gate coupled to the select input of the multiplexer, to an output of the edge detector circuit, and to a memory cell.

14. The circuit according to claim 8 wherein the adjustable delay circuit comprises an odd number of inverting buffers coupled together in series.

15. The circuit according to claim 8 wherein:

the feedback loop is coupled to the input of the adjustable delay circuit when the detect signal is in a first state, and the input of the adjustable delay circuit receives the periodic input signal when the detect signal is in a second state,

the edge-detector circuit causing the detect signal to transition from the first state to the second state, and causing the detect signal to transition from the second state to the first state after one period of the delay signal.

16. A circuit for aligning an input clock signal with a delay signal, the circuit comprising:

means for detecting a phase difference between the input clock signal and the delay signal to generate a phase difference signal;

means for controlling a phase of the delay signal in response to the phase difference signal;

means for detecting edges of the delay signal to generate a detect signal; and

means for selecting the input clock signal or the delay signal as a selected signal in response to a value of the detect signal, wherein the selected signal is delayed by the means for controlling to generate the delay signal.

17. The circuit defined in claim 16 further comprising:

means for dividing a frequency of the delay signal by N to generate a first divided signal, wherein the means for detecting the phase difference between the input clock signal and the delay signal compares the input clock signal to the first divided signal.

18. The circuit defined in claim 17 further comprising:

means for dividing the frequency of the delay signal by M to generate an output clock signal, wherein a frequency of the output clock signal is N/M times the frequency of the input clock signal.

19. The circuit defined in claim 16 further comprising:

means for causing the means for selecting to select the delay signal as the selected signal regardless of the value of the detect signal when a disable signal is a predetermined value.

20. The circuit defined in claim 16 wherein the means for detecting the edges of the delay signal counts falling edges of the delay signal.

21. The circuit defined in claim 16 wherein the means for selecting selects the delay clock signal as the selected signal during a first state of operation, and the means for selecting selects the input clock signal as the selected signal for one period of the delay signal during a second state of operation.

22. The circuit defined in claim 16 wherein the circuit for aligning the input clock signal with the delay signal in part of a field programmable gate array.